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Christian Zebelein

Dr.-Ing. Christian Zebelein



Forschungsgebiete - Dissertation

- A Model-Based Approach for the Specification and Refinement of Streaming Applications

Projekte

- AEOS - Aktororientierte Synthese und Optimierung digitaler Hardware/Software-Systeme auf Systemebene

Lehrveranstaltungen

- Seminar Rechnerarchitektur
- Seminar Simulation und Synthese digitaler Systeme
- Laborpraktikum Softwaretechnik

Publikationen

- Joachim Falk, Christian Haubelt, Jürgen Teich, Christian Zebelein:
SystemoC: A Dataflow Programming Model for Codesign
In Handbook of Hardware/Software Co-Design, Springer, Berlin, Deutschland, Januar 2017 (to appear)
- Joachim Falk, Tobias Schwarzer, Michael Glaß, Jürgen Teich, Christian Zebelein, Christian Haubelt:
Quasi-Static Scheduling of Data Flow Graphs in the Presence of Limited Channel Capacities
In Proceedings of the IEEE Symposium on Embedded Systems for Real-time Multimedia (ESTIMEDIA'15), pp. 29-38, Amsterdam, Niederlande, Oktober 2015
- Tobias Schwarzer, Joachim Falk, Michael Glaß, Jürgen Teich, Christian Zebelein, Christian Haubelt:
Throughput-optimizing Compilation of Dataflow Applications for Multi-Cores using Quasi-Static Scheduling
In Proceedings of the International Workshop on Software and Compilers for Embedded Systems (SCOPES'15), pp. 68 – 75, St. Goar, Deutschland, Juni 2015
- Zebelein, C.; Haubelt, C.; Falk, J.; Schwarzer, T.; Teich, J.
Model-Based Actor Multiplexing with Application to Complex Communication Protocols
In Proceedings of Design, Automation and Test in Europe (DATE'14), pp. 1-4, Dresden, Deutschland, März 2014
- Haubelt, C.; Ludwig, F.; Middendorf, L.; Zebelein, C.
Using Stream Rewriting for Mapping and Scheduling Data Flow Graphs onto Many-Core Architectures
In Proceeding of the Asilomar Conference on Signals, Systems, and Computers, pp. 1431-1435, Pacific Grove CA, USA, November 2013
- Zebelein, C.; Haubelt, C.; Falk, J.; Schwarzer, T.; Teich, J.
Representing Mapping and Scheduling Decisions within Dataflow Graphs
In Forum on specification and Design Languages (FDL), pp. 1-8, Paris, Frankreich, September 2013
- Middendorf, L.; Zebelein, C.; Haubelt, C.
Dynamic Task Mapping onto Multi-Core Architectures through Stream Rewriting
In Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation, pp. 196-204, Samos, Greece, Juli 2013
- Falk, J.; Haubelt, C.; Zebelein, C.; Teich, J.
Integrated Modeling Using Finite State Machines and Dataflow Graphs
In Handbook of Signal Processing Systems, 2nd ed., pp. 975-1013, ISBN: 978-1-4614-6858-5, New York, USA, Juni 2013
- Falk, J.; Zebelein, C.; Haubelt, C.; Teich, J.
A Rule-Based Quasi-Static Scheduling Approach for Static Islands in Dynamic Dataflow Graphs
ACM Transactions on Embedded Computing Systems, ISSN: 1539-9087, Vol. 12, No. 3, pp. 74:1-74:31, DOI: 10.1145/2442116.2442124, New York, U.S.A., April 2013
- Zebelein, C.; Haubelt, C.; Falk, J.; Teich, J.
Model-Based Representation of Schedules for Dataflow Graphs
16. Workshop Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV 2013), pp. 105-116, ISBN: 978-3-86009-147-0, Rostock-Warnemünde, Deutschland, März 2013
- Zebelein, C.; Falk, J.; Haubelt, C.; Teich, J.
A Model-Based Inter-Process Resource Sharing Approach for High-Level Synthesis of Dataflow Graphs
ESLsyn 2012, ISBN: 978-2-9539987-1-9, San Francisco, USA, Juni 2012
- Zebelein, C.; Falk, J.; Haubelt, C.; Teich, J.
Exploiting Model-Knowledge in High-Level Synthesis
15. Workshop für Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen (MBMV'12), pp. 181-191, Kaiserslautern, Deutschland, März 2012
- Falk, J.; Zebelein, C.; Haubelt, C.; Teich, J.
A Rule-Based Static Dataflow Clustering Algorithm for Efficient Embedded Software Synthesis
Design, Automation and Test in Europe, pp. 1-6, ISBN: 978-3-9810801-7-9, Grenoble, France, März 2011
- Falk, J.; Zebelein, C.; Keinert, J.; Haubelt, C.; Teich, J.; Bhattacharyya, S.
Analysis of SystemC Actor Networks for Efficient Synthesis
ACM Transactions on Embedded Computing Systems, New York, U.S.A., Dezember 2010
- Falk, J.; Keinert, J.; Zebelein, C.; Haubelt, C.; Teich, J.
Integrated Modeling Using Finite State Machines and Dataflow Graphs
Handbook of Signal Processing Systems, Rostock, Deutschland, Oktober 2010
- Zebelein, C.; Falk, J.; Haubelt, C.; Teich, J.; Dorsch, R.
Efficient High-Level Modeling in the Networking Domain
Proceedings of Design, Automation and Test in Europe (DATE 2010), Dresden, Germany, März 2010
- Falk, J.; Zebelein, C.; Haubelt, C.; Teich, J.; Dorsch, R.
Integrating Hardware/Firmware Verification Efforts Using SystemC High-Level Models
Tagungsband des 13. ITG/GI/GMM Workshops für Methoden und Beschreibungssprachen zur Modellierung und Verifikation von Schaltungen und Systemen, Dresden, Germany, Februar 2010
- Zebelein, C.; Falk, J.; Haubelt, C.; Teich, J.
Classification of General Data Flow Actors into Known Models of Computation
In Proceedings of the Sixth ACM/IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE2008), pp. 119-128 , Anaheim, CA, USA, Juni 2008

Suchbegriff...



Mitarbeitersuche...



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