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Applied VLSI design (2010)

Phases

Phase 1 (3 weeks)

- Tutors:
- Dipl.-Ing. Andreas Tockhorn
- Dipl.-Ing. Philipp Gorski
- M.Sc. Tim Wegner
- Tasks:
- Get familiar with color space transformation and its operations
- Use the Xilinx FPGA Synthesis tools and the ModelSim simulation environment
- Direct implementation of the color space transformation (do not use + and *-operators): **Source code ma/cc14/teaching/2010_phase1_source_code.zip**, **Slides Meeting 1 ma/cc14/teaching/2010_meeting_1_intro.pdf**
- The target FPGA you have to choose in the Xilinx ISE Project is a Virtex 5 (Family: Virtex5, Device: xc5vfx70t, Package: ff1136, Speed: -1).
- Template and important hints for the presentation of achieved results: **Template Results ma/cc14/teaching/2010_template_results.ppt** (can be used, no must)
- **Target**: Your first working color space transformation design

Phase 2 (3 weeks)

- Tutors:
- Dipl.-Ing. Andreas Tockhorn
- Dipl.-Ing. Philipp Gorski
- M.Sc. Tim Wegner
- Tasks:
- Architectural / Component Optimization (Adders, Multipliers, CSD, Pipelining, parallelization, term sharing, ...)
- Results for the next presentation have to include frequencies for the synthesized and backannotated design (**Slides Meeting 2**)
- The constraint-file **ucf file** can be used to define pin positions and timing constraints for various signals
- **Target**: A better design, in terms of the metric

Phase 3 (3 weeks)

- Tutors:
- Dipl.-Ing. Hagen Sämrow
- Dipl.-Ing. Claas Cornelius
- M.Sc. Martin Gag
- Tasks:
- Mapping on ST65 technology: **Slides Meeting 3 ma/cc14/teaching/2010_meeting_3_synthesis.pdf** **Source archive**
- Further design improvements using the synthesis scripts and tools (architectural changes are welcome but we want to primarily see an adaptation of your design due to the ASIC technology instead of the FPGA and we expect you to purposefully enhance the synthesis scripts for your design requirements)
- Remark: For a correct power simulation, your design hierarchy must be flat!
- **Target**: A working and optimized ST65 netlist
- Chip area is limited to **250000 µm²** (= 500 µm * 500 µm)

Phase 4 (3 weeks)

- Tutors:
- Dipl.-Ing. Hagen Sämrow
- Dipl.-Ing. Claas Cornelius
- M.Sc. Martin Gag
- Tasks:
- Layout for ST65 technology: **Slides Meeting 4 ma/cc14/teaching/2010_meeting_4_layout.pdf** , **Layout sources ma/cc14/teaching/encounter.zip**
- However, investigations and optimizations in all phases are welcome (this is the last phase for the design contest)
- Usage of Cadence First Encounter and Synopsys to achieve backannotated results of a chip layout
- Remark: Your final netlist may not include slashes and backslashes
- Remark: Keep in mind the area limit of maximum side length of 500 µm
- For presentation: Include a picture of your chip layout together with the results (f, P_{dyn}, P_{leak}, A_{core}, Utilization, metric);
- **Target**: Complete ST65 layout and backannotated results

Phase 5 (2 weeks)

- Tutors:
- All involved
- Tasks:
- Investigations on different specific topics have to be performed and presented (for example power distribution, electromigration, pad placement, reliability issues, supply network, clock tree synthesis ...) **Slides Meeting 5 ma/cc14/teaching/2010_meeting_5_topics.pdf**
- **Target**: Deep insight of specific topic and presentation to fellow students
- Evaluation forms will be distributed. Please give us some feedback about the project. All remarks are welcome, e.g.
- Was the project too hard/too easy/just right?
- Was the support by the tutors appropriate and helpful?
- Where would you like the focus to be (hardware, vhdl, architecture ...)?
- Did you learn new content, tools, correlations? If yes, what? What was missing?
- What did you like the most?

Final meeting

- Grades will be posted in front of the secretariat and sent to the student office (ger. Studienbüro)
- Feedback is kindly appreciated. Please return evaluation forms with opinions, criticism, suggestions ...
- A few collected remarks for a quick refresh are included in the **Slides final Meeting ma/cc14/teaching/2010_meeting_6_final.pdf**
- Winner of the design contest is:
- **Best Design:** **Stefan Neumann**
- **MVD - Most Valuable Designer:** **Ralph Erik Sander**
- **Best Presenter:** **Enrico Fentzahn**

Attendees & more

#	Name	Subject	Slides 1st Meeting	Slides 2nd Meeting	Slides 3rd Meeting	Slides 4th Meeting	Slides Final Meeting
1	Enrico Fentzahn	ET	Lorenz_Fentzahn_p1.pdf	Lorenz_Fentzahn_p2.ppt	Fentzahn_p3.ppt	Fentzahn_p4.ppt	Fentzahn_p5.ppt
2	Carsten Lorenz	ET			Lorenz_p3.ppt	Lorenz_p4.ppt	Lorenz_p5.ppt
3	Philipp da Cunha	ET	daCunha_Kutzner_p1.pdf	daCunha_Kutzner_p2.ppt	daCunha_p3.ppt	daCunha_p4.ppt	daCunha_p5.ppt
4	Jonas Kutzner	ET			Kutzner_p3.ppt	Kutzner_p4.ppt	Kutzner_p5.pptx
5	Ralph Erik Sander	ET	Sander_Neumann_p1.pdf	Sander_Neumann_p2.ppt	Sander_p3.ppt	Sander_p4.pptx	Sander_p5.pptx
6	Stefan Neumann	ET			Neumann_p3.ppt	Neumann_p4.ppt	Neumann_p5.pptx
7	Peter Passow	ITTI	Schumacher_Passow_p1.pdf	Schumacher_Passow_p2.ppt	Passow_p3.ppt	Passow_p4.pptx	Passow_p5.pptx
8	Paul Zander	ET	Zander_p1.pdf	Zander_p2.ppt	Zander_p3.pdf		

Latest Results for the Frequency and the Benchmark metrics

#	Name	1st Meeting	2nd Meeting	3rd Meeting	4th Meeting
1	Enrico Fentzahn	60,92 MHz 0,866 Pair*s	484,97 MHz 0,0511 Pair*s	1,80 GHz 1,21e-11 Js	1,02 GHz 1,60e-11 Js
2	Carsten Lorenz			3,00 GHz 1,15e-10 Js	1,13 GHz 2,95e-10 Js
3	Philipp da Cunha	(56,25 MHz) (1,634 Pair*s)	48,36 MHz 1,3304 Pair*s	1,20 GHz 1,51e-12 Js	0,70 GHz 1,63e-12 Js
4	Jonas Kutzner			2,60 GHz 6,45e-13 Js	0,79 GHz 5,37e-13 Js
5	Ralph Erik Sander	**84,78 MHz** **0,283 Pair*s**	**518,94 MHz** **0,0303 Pair*s**	1,07 GHz **2,93e-13 Js**	0,80 GHz 5,85e-13 Js
6	Stefan Neumann			1,77 GHz 3,20e-13 Js	0,75 GHz **5,17e-13 Js**
7	Peter Passow	70,20 MHz 2,303 Pair*s	240,50 MHz 0,2326 Pair*s	2,70 GHz 1,88e-11 Js	**1,53 GHz** 6,46e-12 Js
8	Paul Zander	(87,40 MHz) (0,269 Pair*s)	388,52 MHz 0,0731 Pair*s	**3,45 GHz** 9,94e-12 Js	

Design infos

- Prof. Timmermann Vorlesung **Algorithms in Computer Engineering (Algorithmen der Datentechnik)**
- Prof. Timmermann Vorlesung **VLSI I - Basics of VLSI Technology (Grundlagen der VLSI Technik)**
- Prof. Timmermann Vorlesung **VLSI II - Design of VLSI Systems (Design von VLSI Systemen)**
- Prof. Timmermann Vorlesung **VLSI III - Special Applications of VLSI Design (Spezielle Anwendungen des VLSI Entwurfs)** (former events of this seminar/lecture)
- Brief description of steps from ASIC design to volume production **Design steps**, provided by **Europractice**; see also full **Activity Report 2007**
- **Citeseer**: Huge and uptodate database of scientific papers. Use appropriate keywords for your search.
- **DBLP**: Another database of scientific papers is from the University of Trier.
- **IEEE**: From within the university network, you can search the IEEE proceedings etc...

Arihtmetic structures

- Book „Architekturen der digitalen Signalverarbeitung“, Peter Pirsch
- Book **"Computer Arithmetic: Algorithms and Hardware Designs"**, Behrooz Parhami
  - **Pipelined Algorithms**
- **Booth-Algorithmus**
  - **Booth and modified Booth**
- As Filters mainly consist of Adders and Multipliers, you may find interesting information here:
  - Binary Adder Architectures for Cell-Based VLSI and their Synthesis (**Document**)
  - **Arithmetik**, University of Flensburg
  - Hints for speed freaks:
    - Conditional Sum
      - excellent for speed but needs fast multiplexers
      - in CMOS this can be done using transmission gates
      - however, cascaded transmission gates are slow unless buffers are used
    - Carry Lookahead (CLA)
      - fast, but irregular and large layout, built up of active gates
      - variants of CLA
        - Brent Kung adder
          - small and regular layout, but a bit slow
        - Kogge Stone adder
          - larger but faster
        - Han Carlson adder
          - tradeoff between BK and KS
        - others?
- For everything else: **Google**

Information on Synopsys and ST

- To be able to work with all the tools you need an account for the local laboratories and the general one from the "Rechenzentrum". Please refer to Mrs. Krueger (room 1312) for the local account if you do not have one yet.
- If you want to build the designs out of basic cells you can find the component declarations for Xilinx at $XILINX\vhdl\src\unisims\unisim_VCOMP.vhd on the machine. Consider that not all gates and specialized functions for FPGAs can also be synthesized for an ASIC.
- Use the menu entry "Help->Man pages" for command reference within Synopsys
- Synopsys tutorials, user guides etc. can be found here: /opt/synopsys/synthesis/doc/
- Course info: **Application Specific IC Technology**

Cadence FE

Information on Cadence First Encounter:

- The manual for 2009 can be found here: **Slides Meeting 4**
- The following manuals refer to Silicon Ensemble (previous tool) but are helpful and in part still valid:
- Using the Power Analyzer to evaluate the power consumption: **Power Analyzer**
- **Silicon Ensemble Lecture Slides**
- **Silicon Ensemble Handout**
- A tutorial for the clock tree synthesis: **CTgen-Files**
- A **good tutorial from Lunds University** with additional infos can be found.