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Applied VLSI design (2011)

Phase 1 (3 weeks)

- Tutors:
  - M.Sc. Jan Skodzik
  - M.Sc. Vlado Altmann
  - Dr.-Ing. Claas Cornelius
- Tasks:
  - Get familiar with color space transformation and its operations
  - Use the Xilinx FPGA Synthesis tools and the ModelSim simulation environment
  - Direct implementation of the color space transformation (do not use + and *-operators): **Source code** , **Slides Meeting 1**
  - The target FPGA you have to choose in the Xilinx ISE Project is a Virtex 5 (Family: Virtex5, Device: xc5vfx70t, Package: ff1136, Speed: -1).
  - Template and important hints for the presentation of achieved results: **Template Results** (can be used, no must)
  - **Target**: Your first working color space transformation design

Phase 2 (3 weeks)

- Tutors:
- M.Sc. Jan Skodzik
- M.Sc. Vlado Altmann
- Dr.-Ing. Claas Cornelius
- Tasks:
- Architectural / Component Optimization (Adders, Multipliers, CSD, Pipelining, parallelization, term sharing, ...)
- Results for the next presentation have to include frequencies for the synthesized and backannotated design (**Slides Meeting 2**)
- The constraint-file **ucf file** can be used to define pin positions and timing constraints for various signals
- **Target**: A better design, in terms of the metric

Phase 3 (3 weeks)

- Tutors:
- M.Sc. Martin Gag
- M.Sc. Tim Wegner
- M.Sc. Vlado Altmann
- Tasks:
- Mapping on ST65 technology: **Slides Meeting 3** **Source archive**
- Further design improvements using the synthesis scripts and tools (architectural changes are welcome but we want to primarily see an adaptation of your design due to the ASIC technology instead of the FPGA and we expect you to purposefully enhance the synthesis scripts for your design requirements)
- Chip area is limited to **250000 µm²** (= 500 µm * 500 µm) !!!
- Remark: For a correct power simulation, your design hierarchy must be flat!
- **Target**: A working and optimized ST65 netlist

Phase 4 (4 weeks)

- Tutors:
- M.Sc. Martin Gag
- M.Sc. Tim Wegner
- M.Sc. Vlado Altmann
- Tasks:
- Layout for ST65 technology: **Slides Meeting 4 ma/cc14/teaching/2010_meeting_4_layout.pdf** , **Layout sources ma/cc14/teaching/encounter.zip**
- However, investigations and optimizations in all phases are welcome (this is the last phase for the design contest)
- Usage of Cadence First Encounter and Synopsys to achieve backannotated results of a chip layout
- Remark: Your final netlist may not include slashes and backslashes
- Remark: Keep in mind the area limit of maximum side length of 500 µm
- For presentation: Include a picture of your chip layout together with the results (f, P_{dyn}, P_{leak}, A_{core}, Utilization, metric);
- **Target**: Complete ST65 layout and backannotated results

Phase 5 (2 weeks)

- Tutors:
- All involved
- Tasks:
- Investigations on different specific topics have to be performed and presented (for example power distribution, electromigration, pad placement, reliability issues, supply network, clock tree synthesis ...) **Slides Meeting 5 ma/cc14/teaching/2011_meeting_5_topics.pdf**
- **Target**: Deep insight of specific topic and presentation to fellow students
- Evaluation forms will be distributed. Please give us some feedback about the project. All remarks are welcome, e.g.
- Was the project too hard/too easy/just right?
- Was the support by the tutors appropriate and helpful?
- Where would you like the focus to be (hardware, vhdl, architecture ...)?
- Did you learn new content, tools, correlations? If yes, what? What was missing?
- What did you like the most?

Final meeting

- Grades will be posted in front of the secretariat and sent to the student office (ger. Studienbüro)
- Feedback is kindly appreciated. Please return evaluation forms with opinions, criticism, suggestions ...
- A few collected remarks for a quick refresh are included in the **Slides final Meeting ma/cc14/teaching/2011_meeting_6_final.pdf**
- Winner of the design contest is:
- **Best Design:** **Peter Bartmann**
- **Most Valuable Designer:** **Sebastian Stieber**
- **Certificate of Appreciation:** **Daniel Kern, Michael Rethfeldt**

Attendees & more

#	Name	Subject	Slides 1st Meeting	Slides 2nd Meeting	Slides 3rd Meeting	Slides 4th Meeting	Slides Final Meeting
1	Johann-Peter Wolff	ET	Wolff_Rethfeldt_p1.ppt	Wolff_Rethfeldt_p2.ppt	Wolff_p3.pdf	Wolff_p4.pdf	Wolff_p5.pdf
2	Michael Rethfeldt	IT			Rethfeldt_p3.ppt	Rethfeldt_p4.ppt	Rethfeldt_p5.pdf
3	Benjamin Beichler	IT	Kluwe_Beichler_p1.pdf	Kluwe_Beichler_p2.pdf	Beichler_p3.pdf	Beichler_p4.pdf	Beichler_p5.pdf
4	Alexander Kluwe	IT			Kluwe_p3.pdf	Kluwe_p4.pdf	Kluwe_p5.pdf
5	Björn Konieczek	IT	Gubitz_Konieczek_p1.ppt	Gubitz_Konieczek_p2.ppt	Konieczek_p3.ppt	Konieczek_p4.ppt	Konieczek_p5.ppt
6	Robert Gubitz	IT			Gubitz_p3.ppt	Gubitz_p4.ppt	Gubitz_p5.ppt
7	René Romann	ET	Romann_Haescher_p1.pdf	Romann_Haescher_p2.ppt	Romann_p3.ppt	Romann_p4.ppt	Romann_p5.ppt
8	Marian Haescher	IT			Haescher_p3.pdf	Haescher_p4.pdf	Haescher_p5.pdf
9	Daniel Kern	ET	Bartmann_Kern_p1.pdf	Bartmann_Kern_p2.pdf	Kern_p3.pdf	Kern_p4.pdf	Kern_p5.pdf
10	Peter Bartmann	ET			Bartmann_p3.pdf	Bartmann_p4.pdf	Bartmann_p5.pdf
11	Florian Ludwig	IT	Ludwig_Grunert_p1.ppt	Ludwig_Grunert_p2.ppt	Ludwig_p3.ppt	Ludwig_p4.ppt	Ludwig_p5.ppt
12	Philip Grunert	IT			Grunert_p3.pdf	Grunert_p4.pdf	Grunert_p5.pdf
13	Sebastian Stieber	IT	Kittel_Stieber_p1.ppt	Kittel_Stieber_p2.ppt	Stieber_p3.pdf	Stieber_p4.pdf	Stieber_p5.pdf
14	Martin Kittel	IT			Kittel_p3.ppt	Kittel_p4.ppt	Kittel_p5.ppt
15	Heiko Westphal	IT	Samara_Westphal_p1.ppt	Samara_Westphal_p2.ppt	Westphal_p3.ppt	Westphal_p4.ppt	Westphal_p5.ppt
16	Hani Samara	IT			Samara_p3.ppt	Samara_p4.pdf	Samara_p5.pdf
17	Paul Zander	ET	Zander_p1.pdf	Zander_p2.pdf	Zander_p3.pdf	Zander_p4.pdf	Zander_p5.pdf

Latest Results for the Frequency and the Benchmark metrics

#	Name	1st Meeting	2nd Meeting	3rd Meeting	4th Meeting
1	Johann-Peter Wolff	60.27 MHz 818.85 Pair²*s	60.58 MHz 31.44 Pair²*s	500 MHz, 1680 fJ	90.9 MHz, 708 fJ
2	Michael Rethfeldt			100 MHz, 658 fJ	77.7 MHz, 658 fJ
3	Benjamin Beichler	57.61 MHz 476.00 Pair²*s	254.90 MHz 11.40 Pair²*s	200 MHz, 844 fJ	150.1 MHz, 804 fJ
4	Alexander Kluwe			334.8 MHz, 1130 fJ	206.6 MHz, 2995 fJ
5	Björn Konieczek	77.71 MHz 794.01 Pair²*s	97.38 MHz 38.61 Pair²*s	160 MHz, 572 fJ	148.3 MHz, 672.2 fJ
6	Robert Gubitz			120 MHz, 536 fJ	150.9 MHz, 512 fJ
7	René Romann	41.57 MHz 4205.14 Pair²*s	100.85 MHz 13.49 Pair²*s	500 MHz, 2742 fJ	181.8 MHz, 757 fJ
8	Marian Haescher			300 MHz, 1560 fJ	200 MHz, 657 fJ
7	Daniel Kern	76.89 MHz 450.94 Pair²*s	112.25 MHz **2.06 Pair²*s**	300 MHz, 213 fJ	216 MHz, 288 fJ
8	Peter Bartmann			450 MHz, 176 fJ	392 MHz, **144 fJ**
7	Florian Ludwig	61.67 MHz 952.03 Pair²*s	248.32 MHz 20.50 Pair²*s	100 MHz, 795 fJ	163.8 MHz, 411 fJ
8	Philip Grunert			100 MHz, 1162 fJ	195 MHz, 459 fJ
7	Sebastian Stieber	63.12 MHz 921.58 Pair²*s	133.64 MHz 8.63 Pair²*s	300 MHz, 268 fJ	326.5 MHz, 227 fJ
8	Martin Kittel			244 MHz, 407 fJ	229.5 MHz, 443 fJ
7	Heiko Westphal	38.11 MHz 1928.48 Pair²*s	75.48 MHz 14.73 Pair²*s	150 MHz, 1317 fJ	101.2 MHz, 1074 fJ
8	Hani Samara			250 MHz, 4768 fJ	137.4 MHz, 1130 fJ
7	Paul Zander	**134.33 MHz** **10.79 Pair²*s**	**485.44 MHz** 2.35 Pair²*s	**803.21 MHz**, **133 fJ**	**1490 MHz**, 176 fJ

Design infos

- Prof. Timmermann Vorlesung **Algorithms in Computer Engineering (Algorithmen der Datentechnik)**
- Prof. Timmermann Vorlesung **VLSI I - Basics of VLSI Technology (Grundlagen der VLSI Technik)**
- Prof. Timmermann Vorlesung **VLSI II - Design of VLSI Systems (Design von VLSI Systemen)**
- Prof. Timmermann Vorlesung **VLSI III - Special Applications of VLSI Design (Spezielle Anwendungen des VLSI Entwurfs)** (former events of this seminar/lecture)
- Brief description of steps from ASIC design to volume production **Design steps**, provided by **Europractice**; see also full **Activity Report 2007**
- **Citeseer**: Huge and uptodate database of scientific papers. Use appropriate keywords for your search.
- **DBLP**: Another database of scientific papers is from the University of Trier.
- **IEEE**: From within the university network, you can search the IEEE proceedings etc...

Arihtmetic structures

- Book „Architekturen der digitalen Signalverarbeitung“, Peter Pirsch
- Book **"Computer Arithmetic: Algorithms and Hardware Designs"**, Behrooz Parhami
  - **Pipelined Algorithms**
- **Booth-Algorithmus**
  - **Booth and modified Booth**
- As Filters mainly consist of Adders and Multipliers, you may find interesting information here:
  - Binary Adder Architectures for Cell-Based VLSI and their Synthesis (**Document**)
  - **Arithmetik**, University of Flensburg
  - Hints for speed freaks:
    - Conditional Sum
      - excellent for speed but needs fast multiplexers
      - in CMOS this can be done using transmission gates
      - however, cascaded transmission gates are slow unless buffers are used
    - Carry Lookahead (CLA)
      - fast, but irregular and large layout, built up of active gates
      - variants of CLA
        - Brent Kung adder
          - small and regular layout, but a bit slow
        - Kogge Stone adder
          - larger but faster
        - Han Carlson adder
          - tradeoff between BK and KS
        - others?
- For everything else: **Google**

Information on Synopsys and ST

- To be able to work with all the tools you need an account for the local laboratories and the general one from the "Rechenzentrum". Please refer to Mrs. Krueger (room 1312) for the local account if you do not have one yet.
- If you want to build the designs out of basic cells you can find the component declarations for Xilinx at $XILINX\vhdl\src\unisims\unisim_VCOMP.vhd on the machine. Consider that not all gates and specialized functions for FPGAs can also be synthesized for an ASIC.
- Use the menu entry "Help->Man pages" for command reference within Synopsys
- Synopsys tutorials, user guides etc. can be found here: /opt/synopsys/synthesis/doc/
- Course info: **Application Specific IC Technology**

Cadence FE

Information on Cadence First Encounter:

- The manual for 2009 can be found here: **Slides Meeting 4**
- The following manuals refer to Silicon Ensemble (previous tool) but are helpful and in part still valid:
- Using the Power Analyzer to evaluate the power consumption: **Power Analyzer**
- **Silicon Ensemble Lecture Slides**
- **Silicon Ensemble Handout**
- A tutorial for the clock tree synthesis: **CTgen-Files**
- A **good tutorial from Lunds University** with additional infos can be found.