Navigation
Highlights
Institut
Forschung
Studium und Lehre
Übersicht
Studentische Arbeiten
Hinweise
Mitarbeiter
Presse und Jobs

Quick Links
Publikationen
Anfahrt
Kontakt

Website Info
Suche
Login
Inhalt
Impressum

Login
Benutzer:
Passwort:
LOGIN

Studium und Lehre > Applied VLSI Design 2013

Applied VLSI design (2013)

Official tutors

- **Prof. Dr.-Ing. Dirk Timmermann**
- M.Sc. Vlado Altmann
- M.Sc. Martin Gag
- M.Sc. Jan Skodzik
- M.Sc. Tim Wegner
- **Dr.-Ing. Peter Danielis**

Course info

Schedule: The project **starts on October 16th, 2013** and **ends on January 8th, 2014** (WS 2013/14).
Title: Applied VLSI Design, Module Nr. 24513 (resp. Selected Topics in VLSI Design, Spezielle Anwendungen des VLSI-Entwurfs)

Meetings will take place as scheduled in the **Timetable**, i.e. mostly Wednesday@ 13:00 p.m. in room 1226 (the room and dates may change during the semester, please check on that in advance).

Good and very good grades depend on various aspects like attending ALL meetings, independent and regular work on the given tasks, proper and methodical documentation as well as qualified presentations of achieved results, conclusions and optimizations! Please send all your paper work (docs, hints & advices, slides) and slides to Vlado Altmann **and** Martin Gag Your presentation slides must be sent **1 DAY BEFORE** the scheduled meeting for the presentation! Your work will be added to this website.

As the work is primarily performed in our laboratories, consider the associated general **rules of regulation**.

Presentation

- Each presenter has 5 minutes. The last minute will be indicated. Be aware of your time (5 min), no extra time will be given. Thus, prepare and test your talk at home.
- Accepted file formats are solely ppt and pdf (to avoid conflicts with faulty display do not use latest versions or features that might not be widely supported)
- We want to know:
  - Which problems and room for optimization did you observe in your last design/approach? (with the design, not with the tools)
  - How did you try to tackle the problem(s), what did you expect before starting to investigate (i.e. in theory)?
  - Do your results prove your approach? Why or why not?
- Please do not just copy and paste blurry and skewed images from the literature into your slides. We appreciate self-made diagrams, pictures and sketches. It simply looks better and makes the understanding easier!
- Presentations can be given in GERMAN. However slides have to be prepared in ENGLISH.
- Here, a template for your slides can be downloaded:

2013_template_slides.ppt

Task/Goals for all attendees

- **Given**: Simple, exemplary VHDL description of a filter module (finite impulse response filter, bandpass) and a simple testbench description to simulate and verify the VHDL code of your own filter.
- **Task**: The task is the realization of the same filter functionality as the given one without explicitly using an adder- or multiplier-sign in the VHDL code! The coefficients will be provided. They result in a bandpass behavior of the filter. The goal is to realize a filter with the best metric (depends on phase, see description further down). The winners will be the students with the best metric (for a CORRECTLY WORKING filter, of course).
- **Award**: A nice price will be awarded. More prices and other categories might be awarded depending on the number of students and their work. Awards will be given based on the results for the two different metrics:
  - best design for Xilinx FPGA (metric f^3/(Alut*Aff))
  - best design for ST65 ASIC(metric f^3/(Pdyn*Pleak))

Phase 1 (2 weeks)

- Tutors:
  - M.Sc. Vlado Altmann
  - M.Sc. Jan Skodzik
  - Dr.-Ing. Peter Danielis
- Tasks:
  - Get familiar with filter theory and its operation
  - Use the Xilinx FPGA Synthesis tools and the ModelSim simulation environment
  - Direct implementation of the FIR filter (do not use + and *-operators)
  - The target FPGA you have to choose in the Xilinx ISE Project is a Virtex 6 (Family: Virtex6, Device: xc6vlx240t, Package: ff1156, Speed: -1).
  - Template and important hints for the presentation of achieved results: see below (can be used, no must)
  - **Target**: Your first working FIR filter design

Sources_2013.zip

Meeting1_2013_Intro.pdf

2013_Template_results.ppt

Phase 2 (2 weeks)

- Tutors:
  - M.Sc. Vlado Altmann
  - M.Sc. Jan Skodzik
  - Dr.-Ing. Peter Danielis
- Tasks:
  - Architectural / Component Optimization (Adders, Multipliers, CSD, Pipelining, parallelization, term sharing, ...)
  - Results for the next presentation have to include values for the synthesized and backannotated design
  - The constraint-file (UCF) can be used to define pin positions and timing constraints for various signals
  - **Target**: A better design, in terms of the metric

your_filter.ucf

Meeting2_2013_Optimization.pdf

Phase 3 (2 weeks)

- Tutors:
  - M.Sc. Martin Gag
  - M.Sc. Tim Wegner
  - M.Sc. Vlado Altmann
- Tasks:
  - Mapping on ST65 technology
  - Further design improvements using the synthesis scripts and tools (architectural changes are welcome but we want to primarily see an adaptation of your design due to the ASIC technology instead of the FPGA and we expect you to purposefully enhance the synthesis scripts for your design requirements)
  - Remark: For a correct power simulation, your design hierarchy must be flat (ungroup)!
  - **Target**: A working and optimized ST65 netlist

synopsys.zip

Meeting3_2013_Synthesis.pdf

Phase 4 (2 weeks)

- Tutors:
  - M.Sc. Martin Gag
  - M.Sc. Tim Wegner
  - M.Sc. Vlado Altmann
- Tasks:
  - Layout for ST65 technology
  - However, investigations and optimizations in all phases are welcome (this is the last phase for the design contest)
  - Usage of Cadence Encounter and Synopsys to achieve backannotated results of a chip layout
  - Remark: Your final netlist may not include slashes and backslashes
  - For presentation: Include a picture of your chip layout together with the results (f, P_{dyn}, P_{leak}, A_{core}, Utilization, metric);
  - **Target**: Complete ST65 layout and backannotated results

encounter.zip

Meeting4_2013_Layout.pdf

Phase 5 (1 week)

- Tutors:
  - All involved
- Tasks:
  - Investigations on different specific topics have to be performed and presented (for example power distribution, electromigration, pad placement, reliability issues, supply network, clock tree synthesis ...)
  - **Target**: Deep insight of specific topic and presentation to fellow students
  - Evaluation forms will be distributed. Please give us some feedback about the project. All remarks are welcome, e.g.
    - Was the project too hard/too easy/just right?
    - Was the support by the tutors appropriate and helpful?
    - Where would you like the focus to be (hardware, vhdl, architecture ...)?
    - Did you learn new content, tools, correlations? If yes, what? What was missing?
    - What did you like the most?

Meeting6_2013_Final.pdf

Final meeting

- Grades will be sent to the student office (ger. Studienbüro)
- Feedback is kindly appreciated. Please return evaluation forms with opinions, criticism, suggestions ...
- A few collected remarks for a quick refresh are included in the Slides final Meeting
- Winner of the design contest is:
- **Best Design:** **Christoph Niemann**
- **Most Valuable Designer:** **Vincent Wiese**

Meeting6_2012_Final.pdf

Timetable

Status	Date	Milestone	Description
done	October 16th	Kick-Off Meeting: Start Phase 1	Introduction and start with an exemplary design
done	October 17th	VHDL-Recap	Recapitulation of VHDL, tools and flow
done	October 30th	Intermediate Meeting: Start Phase 2	Initial results for Xilinx, FPGA, VHDL
done	November 13th	Intermediate Meeting: Start Phase 3	Results with backannotated Optimizations for Xilinx, FPGA, VHDL
done	November 27th	Intermediate Meeting: Start Phase 4	Netlist for ST65, results for speed, power, area and the Benchmark Metric from Synopsys tools
done	December 11th	Intermediate Meeting: Start Phase 5	Results from Cadence Tools (First Encounter): Latest improvements, description of best/final architecture, picture of layout, final results on speed, area, power and the benchmark metric
done	January 8th	Final meeting and Dinner	Presentation of individual topics covering chip design (examples may include power distribution, electromigration, pad placement, reliability issues, supply network, clock tree synthesis ...) At ~18.30: Dinner with all attendees, the winners are invited to one dish of their choice. The event will take place in an Restaurant in Rostock

Attendees & slides

#	Name	Group	Slides 1st Meeting	Slides 2nd Meeting	Slides 3rd Meeting	Slides 4th Meeting	Slides Final Meeting
1	Robert Balla	1	G1_P1	G1_P2	1_P3	1_P4	1_P5
2	Henning Puttnies		G5_P1		2_P3	2_P4	2_P5
3	Arne Wall	2	G2_P1	G2_P2	3_P3	3_P4	3_P5
4	Eike Schweißguth				4_P3	4_P4	4_P5
5	Christoph Niemann	3	G3_P1	G3_P2	5_P3	5_P4	5_P5
6	Vincent Wiese				6_P3	6_P4	6_P5
7	Ayad Mostafa	4	G4_P1	G4_P2	7_P3	7_P4	7_P5

Latest results for the frequency and the benchmark metrics

#	Name	1st Meeting	2nd Meeting	3rd Meeting	4th Meeting
1	Robert Balla	*1092.9 MHz (519)*	426 MHz *17.1 MHz^3*	1000 MHz 0.8 e16 MHz^3/W^2	1098 MHz 17.11 e17 MHz^3/W^2
2	Henning Puttnies	*49.4 MHz (0.37)*		**1600 MHz** 39 e16 MHz^3/W^2	1170 MHz 16.68 e17 MHz^3*W^2
3	Arne Wall	*39.619 MHz 0.016 MHz^3*	310 MHz *15.4 MHz^3*	500 MHz 3.3 e16 MHz^3/W^2	**1294 MHz** 3.73 e17 MHz^3/W^2
4	Eike Schweißguth			1119 MHz 79 e16 MHz^3/W^2	1184 MHz 34.54 e17 MHz^3/W^2
5	Christoph Niemann	**53.4 MHz 0.038 MHz^3**	**554 MHz *1460.3 MHz^3***	1111 MHz **206 e16 MHz^3/W^2**	1165 MHz **238.48 e17 MHz^3/W^2**
6	Vincent Wiese			1205 MHz 140 e16 MHz^3/W^2	1093 MHz 12.07 e17 MHz^3/W^2
7	Ayad Mostafa	*229.2 MHz (41.6)*	100 MHz *0.8 MHz^3*	1250 MHz 1.5 e16 MHz^3/W^2	1071 MHz 1.05 e17 MHz^3*W^2

Design infos

- Prof. Timmermann Vorlesung **Algorithms in Computer Engineering (Algorithmen der Datentechnik)**
- Prof. Timmermann Vorlesung **VLSI I - Basics of VLSI Technology (Grundlagen der VLSI Technik)**
- Prof. Timmermann Vorlesung **VLSI II - Design of VLSI Systems (Design von VLSI Systemen)**
- Prof. Timmermann Vorlesung **VLSI III - Special Applications of VLSI Design (Spezielle Anwendungen des VLSI Entwurfs)** (former events of this seminar/lecture)
- Brief description of steps from ASIC design to volume production **Design steps**, provided by **Europractice**; see also full **Activity Report 2007**
- **Citeseer**: Huge and uptodate database of scientific papers. Use appropriate keywords for your search.
- **DBLP**: Another database of scientific papers is from the University of Trier.
- **IEEE**: From within the university network, you can search the IEEE proceedings etc...

Arihtmetic structures

- Book „Architekturen der digitalen Signalverarbeitung“, Peter Pirsch
- Book **"Computer Arithmetic: Algorithms and Hardware Designs"**, Behrooz Parhami
  - **Pipelined Algorithms**
- **Booth-Algorithmus**
  - **Booth and modified Booth**
- As Filters mainly consist of Adders and Multipliers, you may find interesting information here:
  - Binary Adder Architectures for Cell-Based VLSI and their Synthesis (**Document**)
  - **Arithmetik**, University of Flensburg
  - Hints for speed freaks:
    - Conditional Sum
      - excellent for speed but needs fast multiplexers
      - in CMOS this can be done using transmission gates
      - however, cascaded transmission gates are slow unless buffers are used
    - Carry Lookahead (CLA)
      - fast, but irregular and large layout, built up of active gates
      - variants of CLA
        - Brent Kung adder
          - small and regular layout, but a bit slow
        - Kogge Stone adder
          - larger but faster
        - Han Carlson adder
          - tradeoff between BK and KS
        - others?
- For everything else: **Google**

Information on Synopsys and ST

- To be able to work with all the tools you need an account for the local laboratories and the general one from the "Rechenzentrum". Please refer to Mrs. Krueger (room 1312) for the local account if you do not have one yet.
- If you want to build the designs out of basic cells you can find the component declarations for Xilinx at $XILINX\vhdl\src\unisims\unisim_VCOMP.vhd on the machine. Consider that not all gates and specialized functions for FPGAs can also be synthesized for an ASIC.
- Use the menu entry "Help->Man pages" for command reference within Synopsys
- Synopsys tutorials, user guides etc. can be found here: /opt/synopsys/synthesis/doc/
- Course info: **Application Specific IC Technology**

Cadence FE

Information on Cadence First Encounter:

- The following manuals refer to Silicon Ensemble (previous tool) but are helpful and in part still valid:
- Using the Power Analyzer to evaluate the power consumption: **Power Analyzer**
- **Silicon Ensemble Lecture Slides**
- **Silicon Ensemble Handout**
- A tutorial for the clock tree synthesis: **CTgen-Files**
- A **good tutorial from Lunds University** with additional infos can be found.