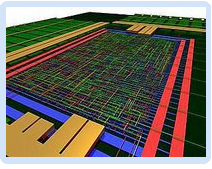
Selected Topics in VLSI Design (2014)

Official tutors

- Prof. Dr.-Ing. Dirk Timmermann
- M.Sc. Vlado Altmann
- M.Sc. Jan Skodzik
- Dr.-Ing. Tim Wegner
- Dr.-Ing. Peter Danielis



Course info

Schedule: The project **starts on October 15th, 2014** and **ends on January 8th, 2015** (WS 2014/15).
Title: Selected Topics in VLSI Design, Module Nr. 24513

Meetings will take place as scheduled in the Timetable, i.e. mostly Thursday@ 11:00 p.m. in room 1226 (the room and dates may change during the semester, please check on that in advance).

Good and very good grades depend on various aspects like attending ALL meetings, independent and regular work on the given tasks, proper and methodical documentation as well as qualified presentations of achieved results, conclusions and optimizations! Please send all your paper work (docs, hints & advices, slides) and slides to Vlado Altmann **and** Tim Wegner. Your presentation slides must be sent **1 DAY BEFORE** the scheduled meeting for the presentation! Your work will be added to this website.

As the work is primarily performed in our laboratories, consider the associated general rules of regulation.

Presentation

- Each presenter has 5 minutes. The last minute will be indicated. Be aware of your time (5 min), no extra time will be given. Thus, prepare and test your talk at home.
- Accepted file formats are solely ppt and pdf (to avoid conflicts with faulty display do not use latest versions or features that might not be widely supported)
- We want to know:
  - Which problems and room for optimization did you observe in your last design/approach? (with the design, not with the tools)
  - How did you try to tackle the problem(s), what did you expect before starting to investigate (i.e. in theory)?
  - Do your results prove your approach? Why or why not?
- Please do not just copy and paste blurry and skewed images from the literature into your slides. We appreciate self-made diagrams, pictures and sketches. It simply looks better and makes the understanding easier!
- Presentations can be given in GERMAN. However slides have to be prepared in ENGLISH.
- Here, a template for your slides can be downloaded: template_slides.ppt

Tasks/goals for all attendees

- **Given**: Simple, exemplary VHDL description of a filter module (finite impulse response filter, highpass) and a simple testbench description to simulate and verify the VHDL code of your own filter.
- **Task**: The task is the realization of the same filter functionality as the given one without explicitly using an adder- or multiplier-sign in the VHDL code! The coefficients will be provided. They result in a highpass behavior of the filter. The goal is to realize a filter with the best metric (see description further down). The winners will be the students with the best metric (for a CORRECTLY WORKING filter, of course).
- **Award**: A nice price will be awarded. More prices and other categories might be awarded depending on the number of students and their work. Awards will be given based on the results for a defined metric:
  - best design for Xilinx FPGA and ST65 ASIC (metric: $f^4/(P_{total})$)

Phase 1 (2 weeks)

- Tutors:
  - M.Sc. Vlado Altmann
  - M.Sc. Jan Skodzik
  - Dr.-Ing. Peter Danielis
- Tasks:
  - Get familiar with filter theory and its operation
  - Use the Xilinx FPGA synthesis tools and the ModelSim simulation environment
  - Direct implementation of the FIR filter (do not use + and *-operators)
  - The target FPGA you have to choose in the Xilinx Vivado Project is a Virtex 7 (Virtex-7 VC707 Evaluation Platform).
  - Template and important hints for the presentation of achieved results: see below (can be used, no must)
  - The constraints-file (.xdc) is required to define a targeted operating frequency for the synthesis tools
  - **Target**: Your first working FIR filter design
- Materials:
  - Meeting1_Intro_2014.pdf
  - VHDL_sources.zip
  - 2014_Template_results.ppt

Phase 2 (2 weeks)

- Tutors:
  - M.Sc. Vlado Altmann
  - M.Sc. Jan Skodzik
  - Dr.-Ing. Peter Danielis
- Tasks:
  - Architectural / component optimization (adders, multipliers, CSD, pipelining, parallelization, term sharing, ...)
  - Results for the next presentation have to include values for the synthesized and backannotated design
  - The constraints-file (.xdc) may be used to define further directives (e.g. for pin positions or timing constraints for various signals)
  - **Target**: A better design, in terms of the metric
- Materials:
  - Meeting2_Optimization_2014.pdf

Phase 3 (2 weeks)

- Tutors:
  - Dr.-Ing. Tim Wegner
- Tasks:
  - Mapping on ST65 technology
  - Further design improvements using the synthesis scripts and tools (architectural changes are welcome but we want to primarily see an adaptation of your design due to the ASIC technology instead of the FPGA and we expect you to purposefully enhance the synthesis scripts for your design requirements)
  - Remark: For a correct power simulation, your design hierarchy must be flat (ungroup)!
  - **Target**: A working and optimized ST65 netlist
- Materials:
  - Meeting3_Synthesis_2014.pdf

Phase 4 (2 weeks)

- Tutors:
  - Dr.-Ing. Tim Wegner
- Tasks:
  - Layout for ST65 technology
  - However, investigations and optimizations in all phases are welcome (this is the last phase for the design contest)
  - Usage of Cadence Encounter and Synopsys to achieve backannotated results of a chip layout
  - Remark: Your final netlist may not include slashes and backslashes
  - For presentation: Include a picture of your chip layout together with the results (f, P_{dyn}, P_{leak}, A_{core}, chip utilization, metric)
  - **Target**: Complete ST65 layout and backannotated results
- Materials:
  - Meeting4_Layout_2014.pdf

Phase 5 (2 weeks)

- Tutors:
  - All involved
- Tasks:
  - Investigations on different specific topics have to be performed and presented (for example power distribution, electromigration, pad placement, reliability issues, supply network, clock tree synthesis ...)
  - **Target**: Deep insight of specific topic and presentation to fellow students
  - Evaluation forms will be distributed. Please give us some feedback about the project. All remarks are welcome, e.g.
    - Was the project too hard/too easy/just right?
    - Was the support by the tutors appropriate and helpful?
    - Where would you like the focus to be (hardware, VHDL, architecture ...)?
    - Did you learn new content, tools, correlations? If yes, what? What was missing?
    - What did you like the most?
- Materials:
  - Meeting5_Topics_2014.pdf

Final meeting

- Grades will be sent to the student office (ger. Studienbüro)
- Feedback is kindly appreciated. Please return evaluation forms with opinions, criticism, suggestions ...
- A few collected remarks for a quick refresh are included in the slides for the final meeting
- Winner of the design contest is:
- **Best Design:** **Kai Neubauer**
- **Most Valuable Designer:** **Lennard Lender**

Timetable

Status	Date	Milestone	Description
done	October 15th	Kick-Off Meeting: Start Phase 1	Introduction and start with an exemplary design
done	October 16th	VHDL-Recap	Recapitulation of VHDL, tools and flow
done	October 30th	Intermediate meeting: Start phase 2	Initial results for Xilinx FPGA
done	November 12th	Intermediate meeting: Start phase 3	Results with backannotated optimizations for Xilinx FPGA
done	November 27th	Intermediate meeting: Start phase 4	Netlist for ST65; results for speed, power, area and the benchmark metric from Synopsys tools
done	December 11th	Intermediate Mmeeting: Start phase 5	Results from Cadence First Encounter, latest improvements, description of best/final architecture; picture of layout; final results on speed, area, power and the benchmark metric
done	January 8th	Final meeting and Dinner	Presentation of individual topics covering chip design (examples may include power distribution, electromigration, pad placement, reliability issues, supply network, clock tree synthesis ...) At ~18:00: Dinner with all attendees, the winners are invited to one dish of their choice. The event will take place in an Restaurant in Rostock

Attendees & slides

Name	Group	1st Meeting	2nd Meeting	3rd Meeting	4th Meeting	Final Meetin
Kai Neubauer	1	Neubauer/Reinartz	Neubauer/Reinartz	Neubauer	Neubauer	Neubau
Tom Reinartz	1			Reinartz	Reinartz	Reinart
Hannes Raddatz	2	Raddatz/Wiedenmann	Raddatz/Wiedenmann	Raddatz	Raddatz	Raddat
Simeon Wiedenmann	2			Wiedenmann	Wiedenmann	Wieder
Nils Büscher	3	Büscher/Lender	Büscher/Lender	Büscher	Büscher	Büsche
Lennard Lender	3			Lender	Lender	Lender

Latest results for the frequency and the benchmark metrics

Name	1st Meeting	2nd Meeting	3rd Meeting	4th Meeting
Kai Neubauer	291 MHz; 2,68*10^10 MHz^4/W	709 MHz; 4,32*10^11 MHz^4/W	3442 MHz; 15,2*10^14 MHz^4/W	4464 MHz; 6,61*10^15 MHz^4/W
Tom Reinartz	291 MHz; 2,68*10^10 MHz^4/W	709 MHz; 4,32*10^11 MHz^4/W	3700 MHz; 15,3*10^14 MHz^4/W	2874 MHz; 6,83*10^14 MHz^4/W
Hannes Raddatz	55 MHz; 2,36*10^7 MHz^4/W	437 MHz; 7,29*10^10 MHz^4/W	3360 MHz; 5,1*10^14 MHz^4/W	3500 MHz; 3,28*10^15 MHz^4/W
Simeon Wiedenmann	55 MHz; 2,36*10^7 MHz^4/W	437 MHz; 7,29*10^10 MHz^4/W	2500 MHz; 3,1*10^14 MHz^4/W	2445 MHz; 7,79*10^14 MHz^4/W
Nils Büscher	150 MHz; 8,52*10^8 MHz^4/W	709 MHz; 4,88*10^11 MHz^4/W	3700 MHz; 17,2*10^14 MHz^4/W	4444 MHz; 5,65*10^15 MHz^4/W
Lennard Lender	150 MHz; 8,52*10^8 MHz^4/W	709 MHz; 4,88*10^11 MHz^4/W	4000 MHz; 32,6*10^14 MHz^4/W	4424 MHz; 3,65*10^15 MHz^4/W

Design infos

- Prof. Timmermann lecture Advanced VLSI Design
- Prof. Timmermann lecture HIS - Highly Integrated Systems (Hochintegrierte Systeme)
- Prof. Timmermann seminar Applied VLSI Design (former events of this seminar)
- Brief description of steps from ASIC design to volume production Design steps, provided by Europractice; see also full Activity Report 2007 (you may also check successive reports for further Information)
- Citeseer: Huge and uptodate database of scientific papers. Use appropriate keywords for your search.
- DBLP: Another database of scientific papers is from the University of Trier.
- IEEE: From within the university network, you can search the IEEE proceedings etc...

Arithmetic structures

- Book „Architekturen der digitalen Signalverarbeitung“, Peter Pirsch
- Book "Computer Arithmetic: Algorithms and Hardware Designs", Behrooz Parhami
  - Pipelined Algorithms
- Booth-Algorithmus
  - Booth and modified Booth
- As Filters mainly consist of Adders and Multipliers, you may find interesting information here:
  - Binary Adder Architectures for Cell-Based VLSI and their Synthesis (Document)
  - Arithmetik, University of Flensburg
  - Hints for speed freaks:
    - Conditional Sum
      - excellent for speed but needs fast multiplexers
      - in CMOS this can be done using transmission gates
      - however, cascaded transmission gates are slow unless buffers are used
    - Carry Lookahead (CLA)
      - fast, but irregular and large layout, built up of active gates
      - variants of CLA
        - Brent Kung adder
          - small and regular layout, but a bit slow
        - Kogge Stone adder
          - larger but faster
        - Han Carlson adder
          - tradeoff between BK and KS
        - others?
- For everything else: Google

Information on Synopsys and ST

- To be able to work with all the tools you need an account for the local laboratories and the general one from the "Rechenzentrum". Please refer to Mrs. Krueger (room 1312) for the local account if you do not have one yet.
- If you want to build the designs out of basic cells you can find the component declarations for Xilinx at $XILINX\vhdl\src\unisims\unisim_VCOMP.vhd on the machine. Consider that not all gates and specialized functions for FPGAs can also be synthesized for an ASIC.
- Use the menu entry "Help->Man pages" for command reference within Synopsys
- Synopsys tutorials, user guides etc. can be found here: /opt/synopsys/synthesis/doc/

Cadence FE

Information on Cadence First Encounter:

- The following manuals refer to Silicon Ensemble (previous tool) but are helpful and in part still valid:
  - Using the Power Analyzer to evaluate the power consumption: Power Analyzer
  - Silicon Ensemble Lecture Slides
  - Silicon Ensemble Handout
  - A tutorial for the clock tree synthesis: CTgen-Files
  - A good tutorial from Lunds University with additional infos can be found.