

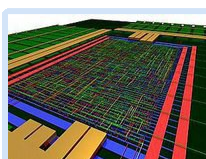
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Selected Topics in VLSI Design (2016)

Official tutors

- Prof. Dr.-Ing. Dirk Timmermann
- M.Sc. Christoph Niemann
- M.Sc. Hannes Raddatz



Course info

Schedule: The project **starts on October 13th, 2016** and **ends on January 12th, 2017** (WS 2016/17).
 Title: Selected Topics in VLSI Design, Module Nr. 24513

Meetings will take place as scheduled in the [Timetable](#), i.e. mostly Thursday@ 11:15 a.m. in room 1218.

Good and very good grades depend on various aspects like attending ALL meetings, independent and regular work on the given tasks, proper and methodical documentation as well as qualified presentations of achieved results, conclusions and optimizations! Please send all your paper work (docs, hints & advices, slides) and slides to [Christoph Niemann](#) and [M.Sc. Hannes Raddatz](#). Your presentation slides must be sent **1 DAY BEFORE** the scheduled meeting for the presentation! Your work will be added to this website.

As the work is primarily performed in our laboratories, consider the associated general [rules of regulation](#).

Presentation

- Each presenter has 5 minutes. The last minute will be indicated. Be aware of your time (5 min), no extra time will be given. Thus, prepare and test your talk at home.
- Accepted file formats are solely ppt and pdf (to avoid conflicts with faulty display do not use latest versions or features that might not be widely supported)
- We want to know:
 - Which problems and room for optimization did you observe in your last design/approach? (with the design, not with the tools)
 - How did you try to tackle the problem(s), what did you expect before starting to investigate (i.e. in theory)?
 - Do your results prove your approach? Why or why not?
- Please do not just copy and paste blurry and skewed images from the literature into your slides. We appreciate self-made diagrams, pictures and sketches. It simply looks better and makes the understanding easier!
- Presentations can be given in GERMAN. However slides have to be prepared in ENGLISH.
- Here, a template for your slides can be downloaded: [template_slides.ppt](#)

Phase 1 (2 weeks)

- Tutors:
 - M.Sc. Christoph Niemann
 - M.Sc. Hannes Raddatz
- Tasks:
 - Get familiar with filter theory and its operation
 - Use the Xilinx FPGA synthesis tools and the ModelSim simulation environment
 - Direct implementation of the FIR filter (do not use + and *-operators)
 - The target Hardware you have to choose in the Xilinx Vivado Project is a Zedboard.
 - Template and important hints for the presentation of achieved results: see below (can be used, no must)
 - The constraints-file (.xdc) is required to define a targeted operating frequency for the synthesis tools
 - **Target:** Your first working FIR filter design
- Materials:

WS16_17_vlsi_1.pdf	715 K
Meeting Slides	
sources2016.zip	642 K
Source Data	
How_to_Setup_your_Project.pdf	192 K
Xilinx Vivado Setup Guide	
vhdl_recap.pdf	496 K
VHDL Quick Guide (short)	
vhdl_quick_guide_full.pdf	1.4 M
VHDL Quick Guide (comprehensive)	

Phase 2 (2 weeks)

- Tasks:
 - Architectural / component optimization (adders, multipliers, CSD, pipelining, parallelization, term sharing, ...)
 - Results for the next presentation have to include values for the **synthesized and backannotated** design
 - The constraints-file (.xdc) may be used to define further directives (e.g. for pin positions or timing constraints for various signals)
 - **Target:** A better design, in terms of the metric
- Materials:

WS16_17_vlsi_2.pdf	470 K
Meeting Slides	
convert_coeffs.m	873
Coefficients Conversion Script	

Attendees & slides

Name	1st Meeting	2nd Meeting	3rd Meeting	4th Meeting	5th Meeting
Sebastian Behl	G1P1				
Jakob Heller	G1P1				
Abhilash G Kammath	G2P1				
Saddam Hussain	G2P1				
Vishnu Raj	G2P1				

Timetable

Status	Date	Milestone	Description
done	October 13th	Kick-Off Meeting: Start Phase 1	Introduction and start with an exemplary design
done	October 17th	VHDL-Recap	Recapitulation of VHDL, tools and flow
canceled	October 27th	Intermediate meeting: Start phase 2	Initial results for Xilinx FPGA
canceled	November 10th	Intermediate meeting: Start phase 3	Results with backannotated optimizations for Xilinx FPGA
canceled	November 24th	Intermediate meeting: Start phase 4	Final FPGA-Design
canceled	December 8th	Intermediate meeting: Start phase 5	Results from Cadence First Encounter, latest improvements, description of best/final architecture; picture of layout; final results on speed, area, Netlist for ST65; results for speed, power, area and the benchmark metric from Synopsys tools
canceled	January 12th	Final meeting	Results from Cadence First Encounter, latest improvements, description of best/final architecture; picture of layout; final results on speed, area, power and the benchmark metric
canceled	January 12th - 18:00	Dinner	

Design infos

- Prof. Timmermann lecture [Advanced VLSI Design](#)
- Prof. Timmermann lecture [HIS - Highly Integrated Systems \(Hochintegrierte Systeme\)](#)
- Prof. Timmermann seminar [Applied VLSI Design \(former events of this seminar\)](#)
- Brief description of steps from ASIC design to volume production [Design steps](#), provided by [Europractice](#); see also full [Activity Report 2014](#) (you may also check successive reports for further information)
- [CiteSeer](#): Huge and up-to-date database of scientific papers. Use appropriate keywords for your search.
- [DBLP](#): Another database of scientific papers is from the University of Trier.
- [IEEE](#): From within the university network, you can search the IEEE proceedings etc...

Arithmetic structures

- Book „Architekturen der digitalen Signalverarbeitung“, Peter Pirsch
- Book "Computer Arithmetic: Algorithms and Hardware Designs", Behrooz Parhami
 - [Pipelined Algorithms](#)
- Booth-Algorithmus
 - [Booth and modified Booth](#)
- As Filters mainly consist of Adders and Multipliers, you may find interesting information here:
 - [Binary Adder Architectures for Cell-Based VLSI and their Synthesis \(Document\)](#)
 - [Arithmetik](#), University of Flensburg
 - [Hints for speed freaks](#):
 - [Conditional Sum](#)
 - excellent for speed but needs fast multiplexers
 - in CMOS this can be done using transmission gates
 - however, cascaded transmission gates are slow unless buffers are used
 - [Carry Lookahead \(CLA\)](#)
 - fast, but irregular and large layout, built up of active gates
 - variants of CLA
 - [Brent Kung adder](#)
 - small and regular layout, but a bit slow
 - [Kogge Stone adder](#)
 - larger but faster
 - [Han Carlson adder](#)
 - tradeoff between BK and KS
 - others?
- For everything else: [Google](#)

Information on Synopsys and ST

- To be able to work with all the tools you need an account for the local laboratories and the general one from the "ITMZ". Please refer to Mrs. Krueger (room 1312) for the local account if you do not have one yet.
- If you want to build the designs out of basic cells you can find the component declarations for Xilinx at [\\$XILINX/vhdl/src/unisims/unisim_VCOMP.vhd](#) on the machine. Consider that not all gates and specialized functions for FPGAs can also be synthesized for an ASIC.
- Use the menu entry "Help->Man pages" for command reference within Synopsys
- Synopsys tutorials, user guides etc. can be found here: [/opt/lehre/vlsi/](#)

Cadence FE

Information on Cadence First Encounter:

- The following manuals refer to Silicon Ensemble (previous tool) but are helpful and in part still valid:
 - [Using the Power Analyzer](#) to evaluate the power consumption: [Power Analyzer](#)
 - [Silicon Ensemble Lecture Slides](#)
 - [Silicon Ensemble Handout](#)
 - A tutorial for the clock tree synthesis: [CTgen-Files](#)
 - A good tutorial from [Lunds University](#) with additional infos can be found.

Hinweise

- [Raumbelegungsplan WM1218](#)

Suchbegriff...

Mitarbersuche...

Lehrstuhl "Rechner in Technischen Systemen"
 Prof. D. Timmermann

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